

# Midterm Exam

(October 13<sup>th</sup> @ 7:30 pm)

Presentation and clarity are very important! Show your procedure!

## PROBLEM 1 (20 PTS)

- Compute the result of the following operations. The operands are signed fixed-point numbers. The result must be a signed fixed point number. For the division, use  $x = 5$  fractional bits.

$\begin{array}{r} 1.0001 + \\ 1.001001 \end{array}$	$\begin{array}{r} 1000.0101 - \\ 1.010101 \end{array}$	$\begin{array}{r} 01.11111 + \\ 0.00001 \end{array}$
$\begin{array}{r} 01.011 \times \\ 1.01101 \end{array}$	$\begin{array}{r} 1.001 \times \\ 1.0101 \end{array}$	$\begin{array}{r} 01.01110 \div \\ 1.011 \end{array}$

## PROBLEM 2 (30 PTS)

- Calculate the result (provide the 32-bit result) of the following operations with single floating point numbers. Truncate the results when required. When doing fixed-point division, use  $x = 4$  fractional bits.

✓ 42FA8000 + C0E00000	✓ 50DAD000 - D0FAD000	✓ 01800000 × FAB80000	✓ 7B390000 ÷ C8C00000
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## PROBLEM 3 (15 PTS)

- Convert the following signed fixed point numbers in format [12 8] to the dual fixed point format 12.8.4.

FX	A.CE	F.EE	C.OB	8.BF	1.0A
DFX					

## PROBLEM 4 (20 PTS)

- Calculate the result of the following operations where the numbers are represented in dual fixed-point arithmetic. Note that the results must be in the same format. Include an overflow bit when necessary.

DFX Format 12.6.4	Result	Overflow	Result	overflow
C0A + C2B			FB9-072	
2CD + 398			F33-CBF	

## PROBLEM 5 (15 PTS)

- Complete the timing diagram of the following iterative unsigned multiplier ( $N = 4, M = 4$ ). Register: *sclr*: synchronous clear. Here, if *sclr* =  $E = 1$ , the register contents are initialized to 0. Parallel access shift register: If  $E = 1$ :  $s_l = 1 \rightarrow$  Load,  $s_l = 0 \rightarrow$  Shift

